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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,310	06/27/2001	Masahito Suzuki	108066-00037	1647

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,310	SUZUKI, MASAHITO	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Response to Amendment

As per the amendments to the independent claims, the examiner does not see any clarification of the claims by the amendments. In fact, the amendments further confuse the issues that the examiner sought to have clarified originally in the first office action. Therefore, in response to this amendment, the examiner will be more specific about the points that are unclear in the claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the terms "serial parallel" and "serial to parallel" are used. Although the terms "serial parallel" (line 4 and line 8) and "serial to parallel" (line 5) appear to be the same, these terms do not seem to be used interchangeably within the claims. It is therefore unclear to the examiner if there is a different meaning to these separate terms, and if so, what that difference is. Therefore, it is requested of the

applicant in response to this office action to clarify the meaning or difference in meaning of these terms.

In lines 6-8 of claim 1, "...a plurality of boundary scan registers which input selectively an output of the input buffer or an input of a test data, holds the input data, and outputs selectively the held input data or an output of the serial parallel conversion circuit,..." this portion of the claim is unclear for the following reasons:

If the conversion circuit takes a serial output from the input buffer (or input terminals), converts the signal to parallel, how does it load the parallel data (as converted) to the serial boundary scan registers?

It is unclear to the examiner if "an input of a test data" (line 7) is the typical test data input (TDI) or another form of test data.

The limitation " holds the input data " in line 7. There is insufficient antecedent basis for this limitation in the claim, as it is unclear which input data is being referenced by "the input data".

It is unclear to the examiner how the serially connected boundary scan registers are connected to the parallel output of the serial parallel conversion circuit (i.e. do each of the parallel outputs connect to a separate boundary scan register, or how does the parallel output load into the serial boundary scan register selectively?).

Claim 1 (lines 6-8) contains a plurality of elements or steps, which are not separated by a line indent. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

(i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

The dependent claims 2-4 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims 1.

As per claim 5, In lines 7-9 of claim 5, "...a plurality of boundary scan registers which selectively input the internal signal or an input of a test data, hold the input data, and selectively output the held input data or an output of the output buffer, ..." this portion of the claim is unclear for the following reasons:

If the conversion circuit takes a serial output from the input buffer (or input terminals), converts the signal to parallel, how does it load the parallel data (as converted) to the serial boundary scan registers?

It is unclear to the examiner if "an input of a test data" (line 8) is the typical test data input (TDI) or another form of test data.

The limitation " holds the input data " in line 8. There is insufficient antecedent basis for this limitation in the claim, as it is unclear which input data is being referenced by "the input data".

It is unclear to the examiner how the serially connected boundary scan registers are connected to the parallel output of the serial parallel conversion circuit (i.e. do each of the parallel outputs connect to a separate boundary scan register, or how does the parallel output load into the serial boundary scan register selectively?).

Claim 5 (lines 7-9) contains a plurality of elements or steps, which are not separated by a line indent. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

The dependent claims 6-8 inherit the 35 U.S.C. 112, second paragraph issues of the independent claim 5.

As per claim 9, line 4, the amended portion "for parallel to serial" is unclear.

Also in claim 9, "...a plurality of boundary scan registers which selectively input the internal signal or an input of a test data, hold the input data, and selectively output the held input data or an output of the parallel serial conversion circuit,..." this portion of the claim is unclear for the following reasons:

If the conversion circuit takes a serial output from the input buffer (or input terminals), converts the signal to parallel, how does it load the parallel data (as converted) to the serial boundary scan registers?

It is unclear to the examiner if "an input of a test data" (line 8) is the typical test data input (TDI) or another form of test data.

The limitation " holds the input data " in line 8. There is insufficient antecedent basis for this limitation in the claim, as it is unclear which input data is being referenced by "the input data".

It is unclear to the examiner how the serially connected boundary scan registers are connected to the parallel output of the serial parallel conversion circuit (i.e. do each

of the parallel outputs connect to a separate boundary scan register, or how does the parallel output load into the serial boundary scan register selectively?).

Claim 9 (lines 7-9) contains a plurality of elements or steps, which are not separated by a line indent. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

The dependent claim 10 inherits the 35 U.S.C. 112, second paragraph issues of the independent claim 9.

Specification

Based on applicant's response, filed 7/26/04, the objection to the specification has been withdrawn.

Response to Arguments

Applicant's arguments filed 7/26/04 have been fully considered but they are not persuasive.

As per applicant's arguments in (paragraph 2 of page 8) the paper filed 7/26/04 states "Applicant respectfully submits that each of claims 1, 5 and 9 recites subject matter that is neither disclosed nor suggested by the cited prior art. In particular, neither Dhong nor Whetsel, taken together or in combination, disclose or suggest at least the limitation of 'a plurality of boundary scan registers which input selectively an output of

the input buffer or an input of a test data, holds the input data, and outputs selectively the held input data or an output of the serial parallel conversion circuit'."

Although applicant attempted to clear up the examiner's initial misunderstanding of the 'serial-parallel' and 'serial parallel' (also parallel-serial) limitations. These attempts to clarify the claimed subject matter brought other issues into question. Therefore, based on the above-listed 35 U.S.C. 112, second paragraph issues, applicant's arguments are not persuasive.

The examiner will therefore maintain the previous 35 U.S.C. 103 rejections as recited in the previous action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhong et al. U.S. Patent No. 6,014,763 in view of Whetsel U.S. Patent No. 6,405,335.

As per claims 1,5, and 9, Dhong et al. substantially teach the claimed circuitry for testing in an integrated circuit, using the steps of transmitting a scan input in parallel from a tester to the integrated circuit, converting the scan input at the integrated circuit from parallel to serial, and passing the serial scan input through scan circuitry of the integrated circuit, to create a serial scan output. The transmitting step includes the steps of transmitting a scan data input in parallel, and transmitting a scan enable input in parallel. If loading the caches through the scan chain is desired, the control signal (cache enable) is also transmitted in parallel. The scan output can further be converted from serial to parallel, and the scan output transmitted in parallel from the integrated circuit to the tester. The transmitting step takes place at a speed of the tester clock signal, but the scan operates at the full operational speed of the device under test. An optional external scan input can be used to run the scan at a lower speed. A bypass mechanism can also be used to skip the actual scan in order to check the scan interface. The scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. At-speed scan testing can be achieved for speeds in excess of 1 GHz. (column 3 lines7-33) Not explicitly disclosed is that the inputs are buffered.

However, in an analogous art, Whetsel teaches an integrated circuit for testing in which the input signal is input to a series of input buffers connected to the individual

scan paths (column 28, lines 45-61). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the input buffer circuitry connected to the scan paths taught by Dhong et al. This would have been obvious as suggested by Whetsel in order to separate the signals to each path and to reduce the power consumption (column 28, lines 36-44) during a scan sequence.

As per claims 2, 3, 6, 7, and 10, Dhong et al. teach that the scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. As further illustrated in FIG. 5, the scan chain is preferably implemented using additional multiplexer input ports to reduce the load on each distributed signal. The scan enable line is fed to multiple inputs of another multiplexer/latch, which splits the signal into different lines that are fed to second-level multiplexer/latches. The outputs of each of the second-level multiplexer/latches can be similarly split to provide another four inputs to four third-level multiplexer/latches. In this manner, 48 identical scan enable outputs can be provided. This tree structure for distributing the scan chain can allow the scan speed to actually exceed the processor's normal operational speed. In a similar manner, another multiplexer/latch can be used as illustrated in FIG. 6, to divide the cache enable signal into two identical signals, one for the instruction cache, and one for the data cache. (Column 5 lines 46-62 and Fig 5 and Fig 6)

As per claims 4, and 8, Whetsel teaches that when the integrated circuit's functional circuitry is configured for testing, all functional registers (flip/flops or latches) in the integrated circuit are converted into scan registers that form the parallel scan paths shown. Also, during test configuration, all combinational logic in the integrated

circuit that was associated with the functional registers remains associated with the scan registers after the conversion. This conversion of an integrated circuit's functional circuitry into scan paths and combinational logic is well known. (column 5 lines 40-49)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cb
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